(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 389 721 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 89313498.1

(22) Date of filing: 22.12.89

(51) Int. Cl.5: H01L 29/788, H01L 21/28, //G11C17/00

(30) Priority: 27.03.89 US 328964

(43) Date of publication of application: 03.10.90 Bulletin 90/40

(84) Designated Contracting States: DE FR GB NL

(71) Applicant: ICT INTERNATIONAL CMOS TECHNOLOGY, INC.
2125 Lundy Avenue
San Jose California 95131(US)

(72) Inventor: Wang, Samuel T.
1084 DiNapoli Drive
San Jose California 95129(US)

(74) Representative: Hardisty, David Robert et al
BOULT, WADE & TENNANT 27 Furnival Street
London EC4A IPQ(GB)

(54) Flash EPROM cell and method of making such cell

(57) A flash EPROM cell is fabricated using a two polysilicon enhancement mode n-channel transistor process. An active transistor region is formed in a silicon substrate (14) by growing a field oxide (16) around the region. A first polysilicon layer is deposited, etched, and oxidised to form an insulated control gate electrode (18). A second polysilicon layer is deposited over the active transistor region and the control gate electrode (18) and then anisotropically etched to remove all of the second polysilicon material except for a filament (20) adjacent to the control gate electrode (18), which forms a floating gate electrode (20). Source and drain regions (10, 12) are formed in the active transistor region with the control gate electrode (18) and the floating gate electrode (20) positioned over the channel region interconnecting the source and drain regions. The cell is programmed by hot electron channel current injection by proper voltage biasing of the control gate electrode (18) and drain (12). The cell can be either symmetrical or asymmetrical depending on the configuration of the floating gate filament electrode (20).

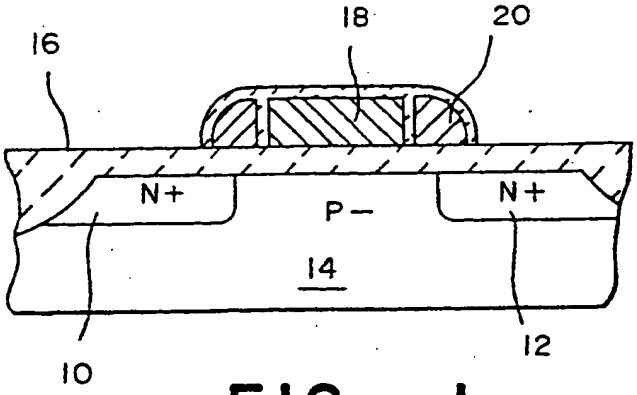

FIG.— 1

EP 0 389 721 A2

This invention relates to a flash EPROM cell and a method of making such cell.

The EPROM cell is an electrically programmable device in which charge is selectively captured on a floating gate positioned between the control gate and the channel region of a field-effect transistor. In programming the floating gate, hot electron channel current injection results from applying a high voltage on the control gate and the drain of the transistor. Electrons from the channel current are injected to the floating gate and cause V_t of the transistor to increase. A programmed EPROM cell is erased by applying ultraviolet light to the cell. Therefore, packaged EPROM cells require a window in the package for illuminating the cell with ultraviolet light.

The EEPROM cell is electrically programmable and electrically erasable. A thin oxide layer is provided between a floating gate and either the source of drain electrode to permit the tunnelling of electrons through the oxide layer for programming and erasing the cell. However, while the EEPROM cell obviates the need for ultraviolet light radiation for erasure, the cell structure is larger due to the need for a select transistor cascoded to the memory transistor for proper bit erasure.

Flash EEPROM structures are known in which an entire memory array can be erased at the same time during an erase operation. Electron tunnelling is employed in the erasing of the cells. The need for a thin tunnelling oxide layer as well as the use of split gate structures in which the control gate overlaps the floating gate leads to production yield problems as well as increased cell size.

According to the invention there is provided a flash EPROM cell comprising a semiconductor body having a surface region of one conductivity type, first and second doped regions of opposite conductivity type formed in said surface region, said first and second regions being spaced and forming source and drain regions of said cell with the surface region therebetween forming a channel region of said cell, an insultative layer over said channel region, a control gate contact positioned on said insulative layer between said source and drain regions, and a floating gate contact positioned on said insulative layer between said source and drain regions, said floating gate contact being spaced from and generally coplanar with said control gate contact and overlapping at least one of said source and drain regions.

Also according to the invention there is provided a method of making a flash EPROM cell, comprising the steps of:-

a) defining an active transistor region in the surface of a semiconductor body of a first conductivity type;

b) forming an insulative layer over the surface of said active transistor region;

c) forming a control gate electrode on said insulative layer in an intermediate portion of said active transistor region;

d) forming an insulative layer over said control gate electrode;

e) forming a floating gate electrode adjacent to and generally coplanar with said control gate electrode on said insulative layer; and

f) forming source and drain regions in said active transistor region, said source and drain regions being spaced apart by a channel region, said control gate electrode and said floating gate electrode overlying said channel region.

The invention provides a flash EPROM cell in which programming and erasure do not require a tunnelling oxide layer.

Briefly a flash EPROM cell is made by forming a control gate structure from a first doped polysilicon material over an active transistor region in a semiconductor body. The control gate in the first polysilicon layer is defined by selective etching and then the surface of the control gate is insulated by an oxide, for example. A second doped polysilicon layer is then formed over the active transistor region and over the insulated control gate structure. Importantly, the second polysilicon layer is thicker around the edges of the control gate structure. Consequently, the second polysilicon layer can be etched by anisotropic etchant or reactive ion etch to remove the second polysilicon material above the control gate structure while a portion of the second polysilicon material remains around the periphery of the control gate structure. This remaining portion becomes a coplanar filament floating gate for use in programming the cell.

Thereafter, the source and drain regions are formed by introducing dopants into the active region adjacent to the filament floating gate structure. Subsequent heat treatment causes diffusion of the dopants under a portion of the filament electrode so that the filament floating gate overlies at least one of the source and drain regions.

In one embodiment, the filament is around the periphery of the control gate on both the source and drain sides and the structure is symmetrical in structure. In another embodiment, the filament floating gate is retained on only one side of the control gate and the structure is asymmetrical. If the filament is on both sides of the control gate, the filament can be connected by a conductive bridge over the control gate, thereby allowing READ and PROGRAM control from the same side and obviating the need for drain/source switching.

In forming the source and drain regions, preferably both arsenic and phosphorus n-type dopants are introduced into the active regions. By using a higher concentration of arsenic than phosphorus,

the faster-diffusing phosphorus will form a more gradual dopant profile with the p- doped channel region. This provides a higher junction breakdown voltage and facilitates the requisite gate-assisted breakdown needed to erase a cell.

The resulting structure has the control gate electrode and the floating filament gate electrode in series across the channel region between the source and drain of the memory transistor. When a cell is programmed as a "1" to conduct current upon application of a READ voltage to the control gate, the filament gate will be charged to effect a depletion mode int he underlying channel region. However, the channel region under the control gate is still in enhancement mode and no leakage current flows between the source and drain except during a READ cycle. Conversely, when the cell is programmed as a "0" with no current flow during a READ cycle, charge on the floating filament electrode prevents conduction across the channel between the source and drain during a READ cycle.

In the symmetrical structure, the programming of a cell entails hot electron channel current injection by applying high voltage on the control gate (e.g. +12 V) and on the drain (e.g. +7 V) while the source is grounded. Electrons from the channel current are injected to the floating filament electrode and cause V_t of the transistor to go high. Thus the cell is non-conductive during a READ cycle.

Erasing of the cell is done by hole injection in a gate-assisted avalanche breakdown mode. The control gate is grounded and the source (or drain) is biased at +7 V while the drain (or source) is biased at 15+ V. The +7V on one element is encessary to avoid the device experiencing punch-through by +15V on the other element. This causes the floating filament electrode to be charged by positive holes, thus rendering the channel region under the filament electrode to be in depletion mode. Erasure can be done on selected cells allowing the design feature of "byte erase".

With the asymmetrical structure, the source and drain electrodes must be reversed during the programming and READ modes. However, the asymmetric structure permits a virtual ground design with the cells arranged as an "X" array.

The invention will now be described by way of example with reference to the drawings, in which:-

Fig. 1 is a sectional view of a flash EPROM transistor cell in accordance with one embodiment of the invention;

Fig. 2 and Fig. 3 are alternative top views of the cell of Fig. 1;

Fig. 4 is an electrical schematic of the cell of Fig. 1;

Fig. 5 is a portion of a memory array using the cell of Fig. 1;

Figs. 6A-6L are sectional views illustrating steps in fabricating the cell of Fig. 1;

Fig. 7 is a sectional view of another embodiment of a flash EPROM cell in accordance with the invention;

Fig. 8 is a top view of the cell of Fig. 7;

Fig. 9 is an electrical schematic of the cell of Fig. 7; and

Fig. 10 is a plan view of a portion of a memory array using the cell of Fig. 7.

Referring now to the drawings, Fig. 1 is a sectional view of one embodiment of a flash EPROM transistor cell in accordance with the invention. The cell comprises an enhancement-mode field-effect transistor having n- source region 10 and an n+ drain region 12 fabricated in a p-substrate 14. A silicon oxide layer 16 is formed on the surface of the substrate 14 above the source 10 and drain 12. A polysilicon control gate 18 is provided on the oxide layer 16 between the source and drain regions, and a polysilicon filament floating gate electrode 20 is formed around the periphery of the control gate 18 and overlaps the source 10 and drain 12, as illustrated.

Fig. 2 is a plan view of the cell of Fig. 1 in accordance with one embodiment, in which the filament electrode 20 completely surrounds the periphery of the control electrode 18 with the filament electrode 20 overlapping the source 10 and drain 12, illustrated in dotted lines. The control gate 18 is formed in a first polysilicon layer (poly 1) 22 which interconnects other control gates in one column of an array of such cells.

Fig. 3 is an alternative plan view of the cell of Fig. 1 in which the floating filament electrode 20 is formed on either side of the control gate 18 and overlaps the source 10 and drain 12. In this embodiment the two portions of the filament electrode 20 are interconnected by a conductive bridge 24 over the control gate 18. The width of the bridge can be the same as the filaments, and the bridge width will change the programming efficiency.

As will be described more fully below with reference to Figs. 6A-6L, the control electrode 18 and the floating gate electrode 20 can be fabricated in a dual polycrystalline silicon process in which the control gate is formed from a first polysilicon layer and the floating filament electrode for programming the cell is fabricated from a second polysilicon layer. The control electrode and the portions of the floating electrode are generally coplanar and are not overlapping, except for the bridge 24 in the embodiment of Fig. 3.

Fig. 4 is an electrical schematic of the cell of Fig. 1 in which the portions of the floating gate electrode 20 and the control gate electrode 18 effectively form three serially-connected channel regions between the source and drain as illustrated.

The serial enhancement transistor prevents current flows between the drain and source when the gate is grounded. Accordingly, when the cell is programmed for a "1", there is no leakage current when the cell is not being read.

Fig. 5 is a plan view of a portion of a memory array using the flash EPROM cell structure of Fig. 1. It will be noted that the polysilicon 1 layers are formed in vertical columns with the control gates of all transistors in each column being interconnected by the poly 1 layer. The source regions of adjacent transistors are interconnected by common n+ source lines as illustrated. The drains of all transistors in horizontal rows are interconnected by metallization (not shown).

In programming the flash EPROM cells of Fig. 1, hot electron channel current injection to the floating gate 20 is effected by applying a high voltage (e.g. 12 volts) to the control gate 18 and a high voltage (e.g. +7 volts) to the drain 12 with the source 10 allowed to float. The symmetrical structure allows the source and drain to be interchanged in the programming, READ and erase modes. Electrons from the channel current are injected to the Poly 2 filament and cause the V_t of the Poly 2 filament channel regions to go high. Since the cell has the Poly 2 filament transistors in series with the Poly 1 control gate transistor, the V_t of the cell becomes high and the cell is in an "off" state ("0" stored).

Erasing of the cell is done by hole injection in a gate-assisted breakdown mode. The control gate 18 (Poly 1) is grounded and the source 10 (or drain 12) is biased at 7 volts with the drain 12 (or source 10) biased to more than 15 volts. This causes the filament Poly 2 electrodes to be charged by positive holes, forcing the Poly 2 filament channel regions to a depletion mode. However, the V_t of the cell is limited by the V_t of the series Poly 1 control gate electrode enhancement transistor, thus preventing the cell from going to a depletion mode. The V_t of the transistor is low in this mode with the transistor programmed as a "1".

The cell structure of Fig. 1 is readily fabricated using a standard polysilicon process employing a Poly 1 layer and a Poly 2 layer. Figs. 6A-6L are sectional views illustrating steps in the fabrication of the flash EPROM transistor cell of Fig. 1.

Initially, as shown in Fig. 6A, a 20 ohm-cm p^- type silicon substrate 30 is provided. In Fig. 6B a silicon oxide layer 31 and a silicon nitride layer 32 are formed on the surface of the substrate 30. Next, in Fig. 6C, the active regions of transistors are masked by photoresist 33, the nitride layer 32 and the oxide layer 31 then being removed thereby exposing portions of the substrate 30. In Fig. 6D, a field implant region and a field oxidation region 35 is formed in the exposed surface areas of the substrate 30 in accordance with standard processing techniques.

Thereafter, in Fig. 6E, a boron implant region 36 is formed in the active transistor regions of the substrate to adjust V_t to 0.5 volt. The oxide is then stripped from above the active transistor region and the gate oxide is regrown. A first doped polysilicon layer 37 is formed over the surface of the substrate and then etched as shown in Fig. 6G to form the control gates 38 and oxidised as shown at 39 in Fig. 6H to form the control gate electrodes of the transistor structures.

Thereafter, as shown in Fig. 1 6I, a second doped polysilicon (Poly 2) layer 40 is deposited by chemical vapour deposition (CVD) over the surface of the substrate and over the control gate 38 with the oxide 39 electrically insulating the Poly 2 layer from the gate electrode 38. The Poly 2 layer is thicker around the periphery of the Poly 1 lines and the control electrodes 38 due to the conforming nature of the CVD deposition.

An anisotropic reactive ion plasma etch (RIE) is employed to remove the Poly 2 layer from over the control electrodes. However, the etch is limited in time so that the thicker Poly 2 layer around the periphery of the control electrode 38 remains as shown at 41 in Fig. 6J. This remaining Poly 2 layer becomes the filament floating gate electrode 20 of the cell. In Fig. 6K, a second mask is employed to remove the Polysilicon 2 layer 40 between the adjacent transistors along the Poly 1 strips interconnecting gate electrodes of adjacent transistors.

Finally, the source and drain regions are formed in the active transistor areas by implantation and subsequent diffusion of two n-type dopants, arsenic and phosphorus. The concentration of arsenic is greater than the concentration of phosphorus, and in a subsequent heat treatment following the implantation of the arsenic and phosphorus, the phosphorus diffuses faster and causes a dopant concentration profile as illustrated in Fig. 6L. The arsenic comprises the n+ region of the source and drain and the phosphorus comprises the n- portion of the source and drain. The lateral diffusion of the phosphorus causes overlap of the source and drain regions with the filament electrodes, as is necessary in programming and erasing each transistor cell. Further, the dopant concentration profile provided by the n+ arsenic and n- phosphorus regions permits higher gate-assisted breakdown for erasing a programmed transistor. As noted above, voltages as high as 15 volts are necessary for effecting the gate-assisted breakdown for flash erase, and the dopant profile permits the p-n junction between the source and drain contacts with the n- channel region to withstand the high reverse bias voltage. An abrupt n+/p- junction could not withstand the high voltages and would

break down at 10-12 volts.

The symmetrical structure of the flash EPROM cell illustrated in Fig. 1 permits programming and erasing of the cell from either the source or drain of the transistor. However, an asymmetrical cell structure can be provided by retaining the polysilicon 2 [Poly 2] filament on only one side of the control gate electrode. This is illustrated in the side view of an alternative embodiment of Fig. 7. In this embodiment the n+ source 50 and n+ drain 51 are again formed in a p- substrate 52 with the control gate electrode 54 formed by Poly 1 material and the floating filament electrode 56 formed by a Poly 2 layer similar to the structure of Fig. 1. However, the Poly 2 is removed by etchant except from the one side of the control gate electrode.

Fig. 8 is a plan view of the cell and shows the filament electrode 56 provided on only one side of the control gate electrode 54 and overlapping only the drain 51. Fig. 9 is an electrical schematic in which the Poly 1 control gate electrode 54 and the Poly 2 filament electrode 56 control serially-connected portions of the channel region between the source and drain.

In this asymmetrical cell structure, the source and drain electrodes must be interchanged between a READ mode and a programming or erase mode. Accordingly, the cells of memory array are preferably aligned in an "X" matrix as shown in Fig. 10. During programming, 7 volts are applied to the drain, 12 volts are applied to the control gate, and the source is grounded for the selected cell while the source is allowed to float for the non-selected cells. This injects electrons to the floating filament electrode and raises the V_t of the underlying channel region. Other non-selected cells have either floating source line or filament on the source side and are not affected by this operation. During an erase operation, the drain is raised to 23 volts, the control gate is grounded, and the source is allowed to float. Hole injection to the floating electrode occurs by gate-assisted avalanche breakdown. During a READ operation, the drain is grounded, 1 volt is applied to the source, and 3 volts are applied to the control gate. If the cell is programmed for a "0" (no current flow), the V_t of the transistor will be 4+ volts. On the other hand, if the cell is programmed for a "1" (current flow), V_t is 0.5 volt.

There has been described a flash EPROM cell which is small in structure (as compared with an EEPROM cell) in which a polysilicon 1 material forms a control gate and a polysilicon 2 layer, generally coplanar with polysilicon 1 layer, forms a floating filament gate electrode. Since the channel regions underlying the control gate and the filament gate are in series, the transistor cell cannot go to a depletion mode even when the floating gate is in a depletion mode. In the symmetrical cell structure, the drain and source regions need not be reversed between programming mode and a READ mode. Importantly, programming of the cell is accomplished by hot electron channel current injection and erasure is accomplished by gate-assisted breakdown hole injection. No tunnelling oxide is required, thus simplifying the fabrication process.

Claims

1. A flash EPROM cell comprising a semiconductor body having a surface region of one conductivity type, first and second doped regions of opposite conductivity type formed in said surface region, said first and second regions being spaced and forming source and drain regions of said cell with the surface region therebetween forming a channel region of said cell, an insultative layer over said channel region, a control gate contact positioned on said insulative layer between said source and drain regions, and a floating gate contact positioned on said insulative layer between said source and drain regions, said floating gate contact being spaced from and generally coplanar with said control gate contact and overlapping at least one of said source and drain regions.

2. A cell as claimed in Claim 1, wherein said control gate contact is formed from a first doped polycrystalline silicon layer and said floating gate contact is formed from a second doped polycrystalline silicon layer.

3. A cell as claimed in Claim 1 or Claim 2, wherein said floating gate contact is adjacent to opposing sides of said control gate contact.

4. A cell as claimed in Claim 3, wherein said floating gate contact overlaps both of said source region and said drian region, said cell being symmetrical in structure and in application.

5. A cell as claimed in Claim 4, wherein said floating gate contact at least partially surrounds the periphery of said control gate contact.

6. A cell as claimed in Claim 4, wherein said floating gate contact includes a bridge portion over said control gate contact which interconnects said floating gate contact on opposing sides of said control gate contact.

7. A cell as claimed in any preceding claim, wherein at least one of said source region and said drain region includes different concentrations of dopants of said opposite conductivity type.

8. A cell as claimed in Claim 7, wherein said concentrations of dopants include arsenic forming an n+ dopant concentration and phosphorus forming an n- dopant concentration.

9. A cell as claimed in Claim 11 or Claim 2, wherein said floating gate contact is adjacent to

one side of said control gate contact and overlaps said drain region.

10. A method of making a flash EPROM cell, comprising the steps of:-

a) defining an active transistor region in the surface of a semiconductor body of a first conductivity type;

b) forming an insulative layer over the surface of said active transistor region;

c) forming a control gate electrode on said insulative layer in an intermediate portion of said active transistor region;

d) forming an insulative layer over said control gate electrode;

e) forming a floating gate electrode adjacent to and generally coplanar with said control gate electrode on said insulative layer; and

f) forming source and drain regions in said active transistor region, said source and drain regions being spaced apart by a channel region, said control gate electrode and said floating gate electrode overlying said channel region.

12. A method as claimed in Claim 10 or Claim 11, wherein step f) includes introducing arsenic and phosphorus into at least said drain region, said arsenic forming an n+ region and said phosphorus forming an n- region.

13. A method of making a flash EPROM cell in a silicon body comprising the steps of:-

a) defining an active transistor region in said silicon body by growing a field silicon oxide layer around the active transistor region;

b) growing a silicon oxide layer over said active transistor region;

c) depositing a first doped polysilicon layer over said active transistor region;

d) etching said first doped polysilicon layer to form a control gate electrode in an intermediate portion of said active transistor region;

e) oxidising the surface of said control gate electrode;

f) depositing a second doped polysilicon layer over said active transistor region and over said control gate electrode;

g) removing said second doped polysilicon layer by etching except adjacent to at least one side of said control gate electrode thereby forming a floating gate electrode adjacent to said control gate electrode; and

h) forming source and drain regions in said active transistor region, said source and drain regions being spaced apart by a channel region, said control gate electrode and said floating gate electrode overlying said channel region.

14. A method as claimed in Claim 13, wherein step g) forms a floating gate electrode on opposing sides of said control gate electrode.

15. A method as claimed in Claim 14, wherein said floating gate electrode is around the periphery of said control gate electrode.

16. A method as claimed in Claim 13, wherein step g) forms a floating gate electrode on only one side of said control gate electrode.

17. A method as claimed in any one of Claims 13 to 16, wherein step h) includes introducing arsenic and phosphorus into at least said drain region, said arsenic forming an n+ region and said phosphorus forming an n- region.

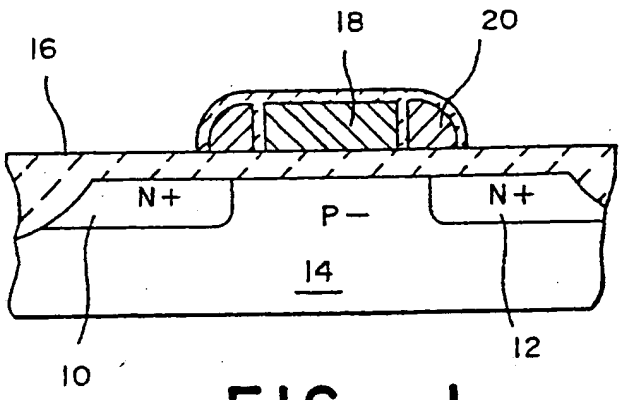

FIG.— 1

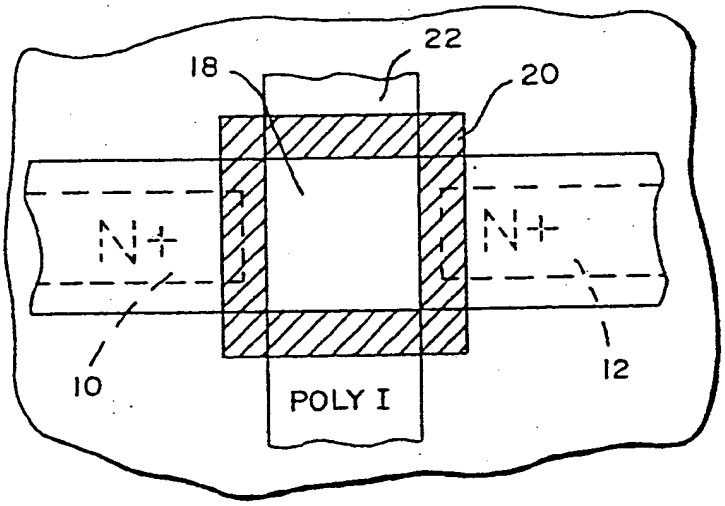

FIG.— 2

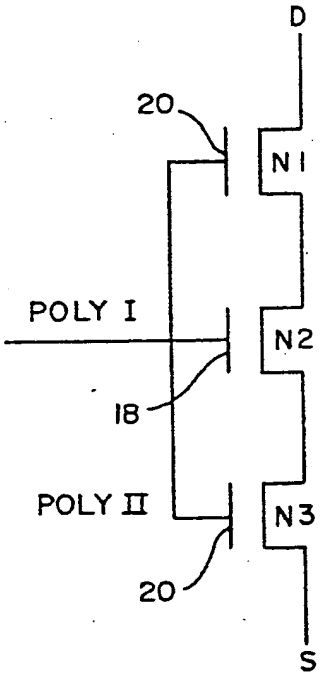

FIG.— 4

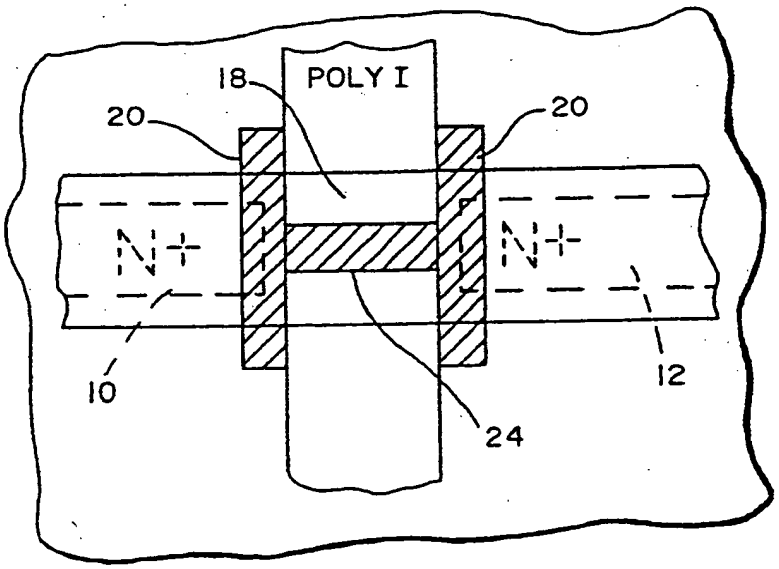

FIG.— 3

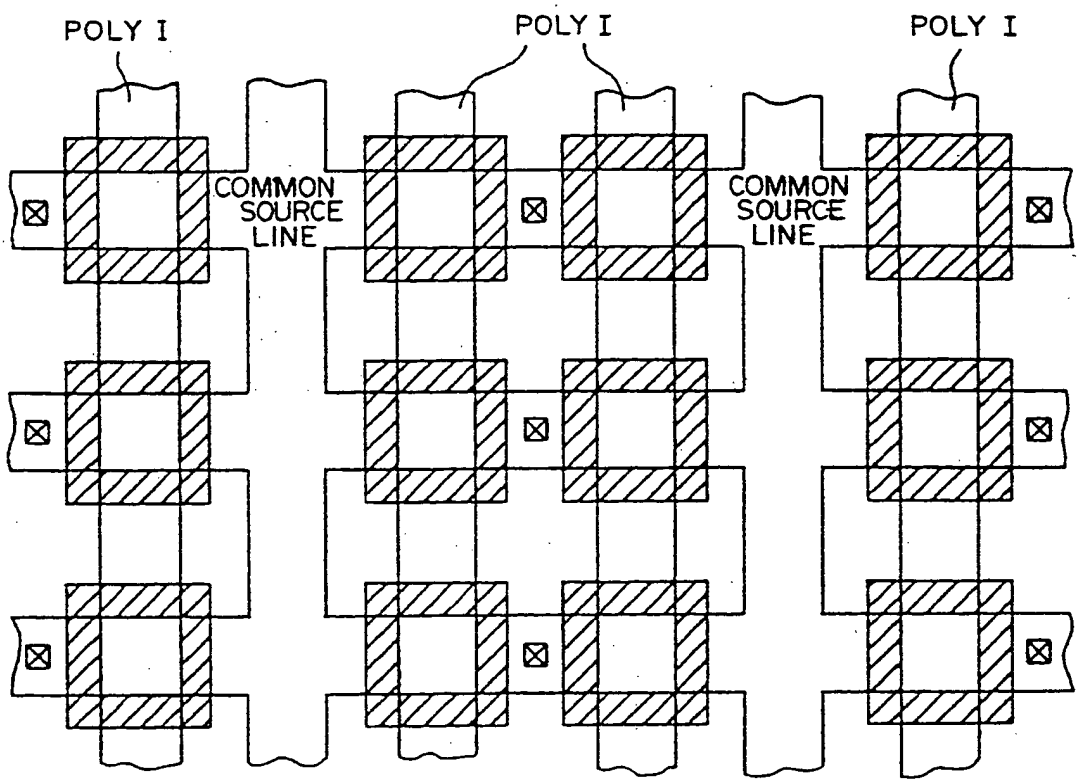

FIG.— 5

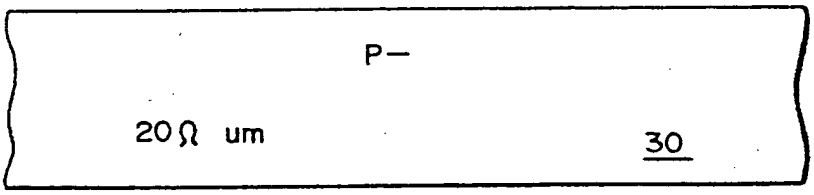

FIG.— 6A

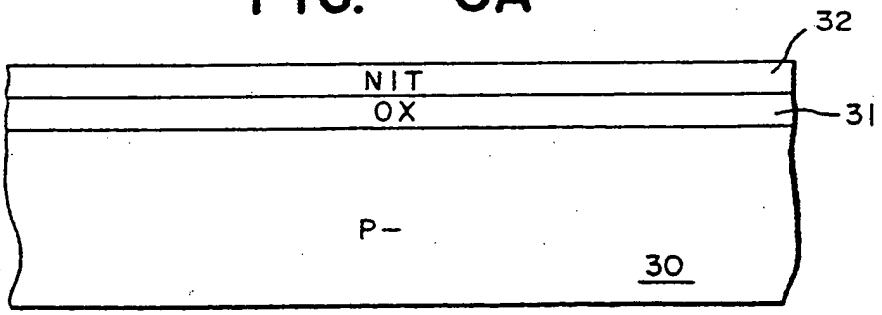

FIG.— 6B

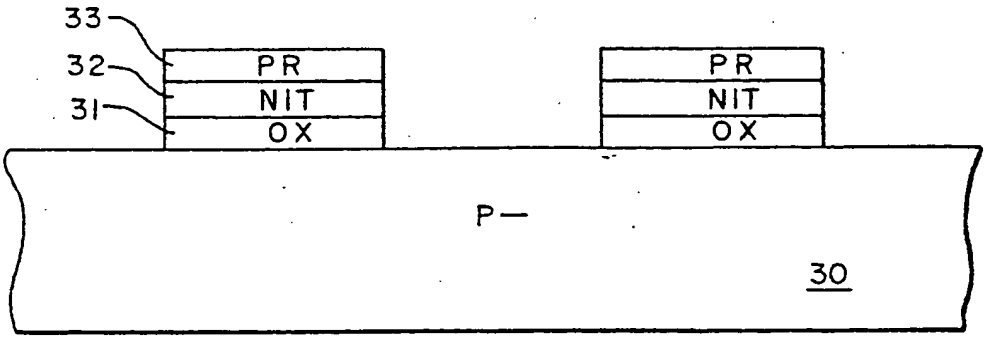

FIG.—6C

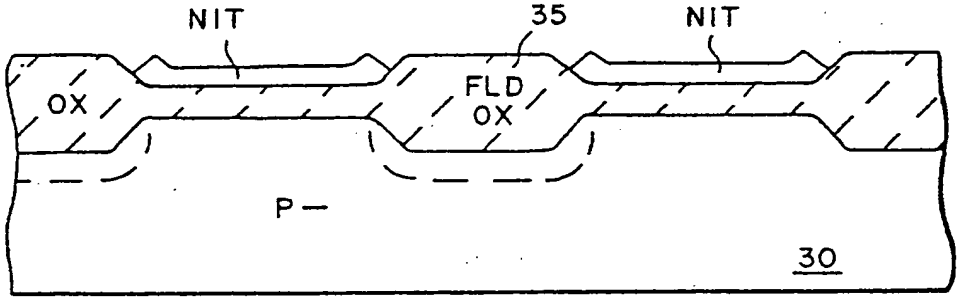

FIG.—6D

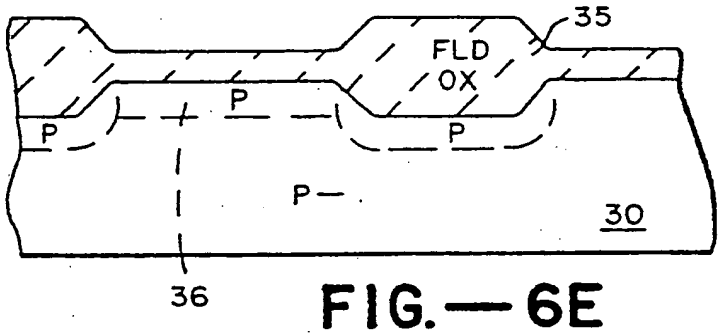

FIG.—6E

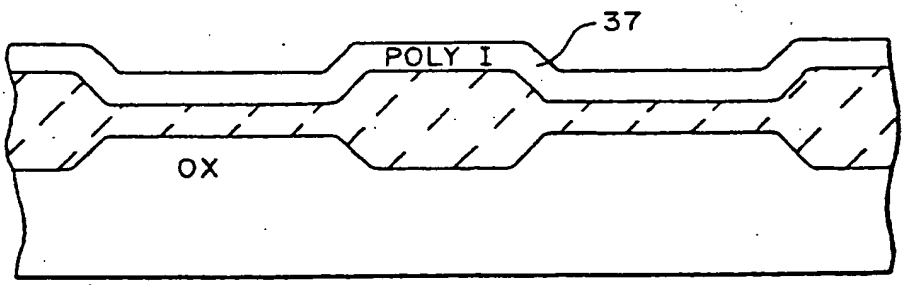

FIG.—6F

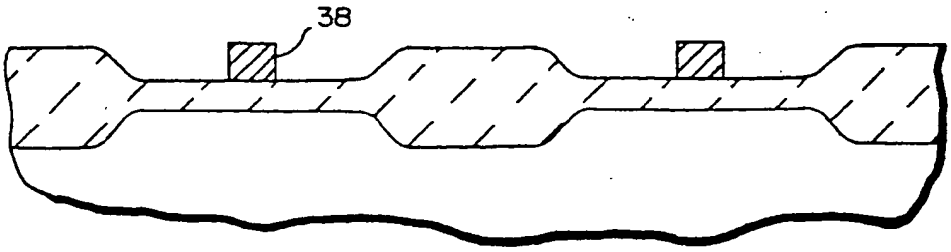

FIG.— 6G

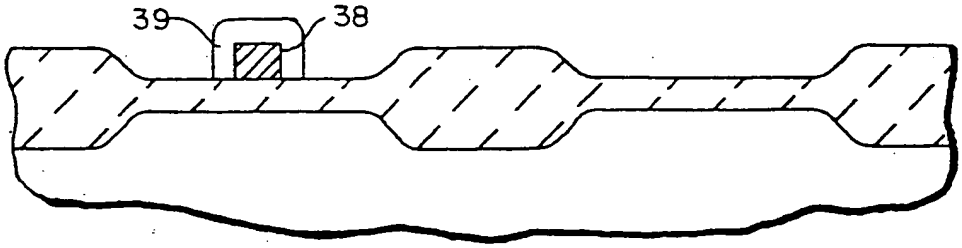

FIG.— 6H

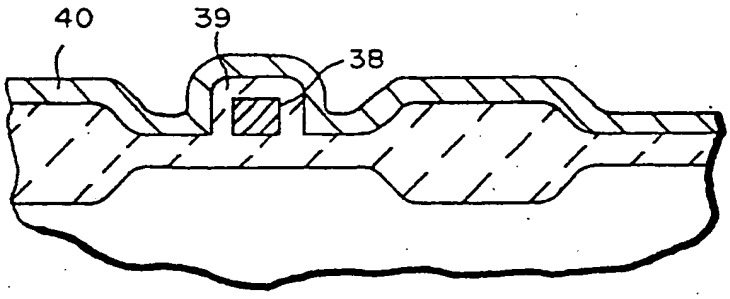

FIG.— 6I

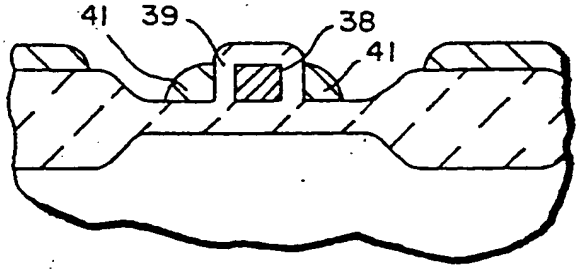

FIG.— 6J

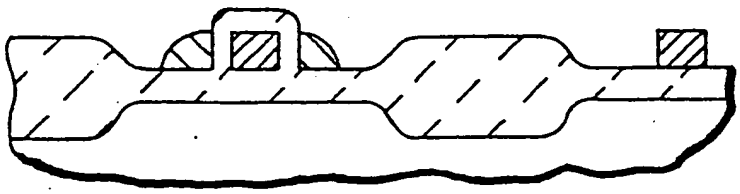

FIG.— 6K

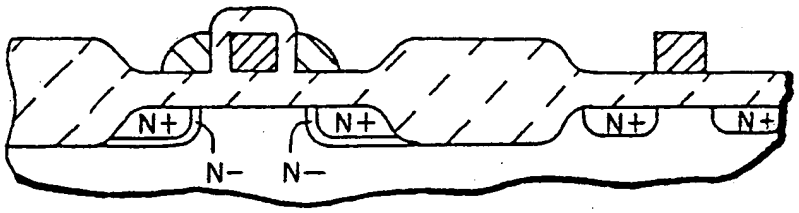

FIG.— 6L

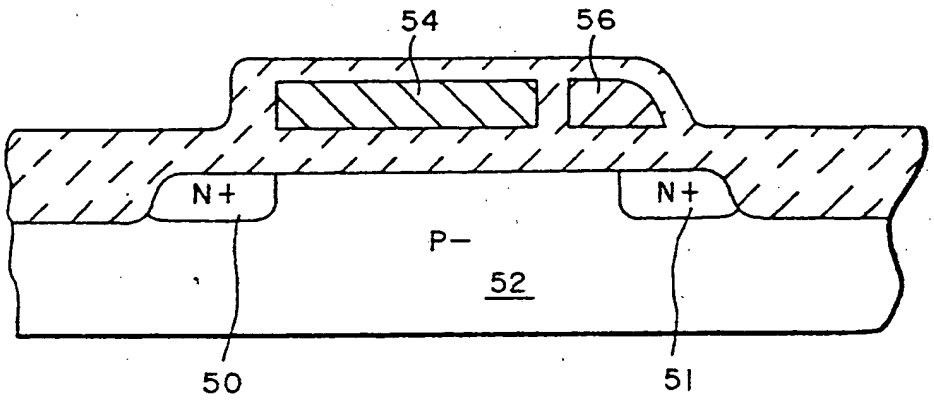

FIG.— 7

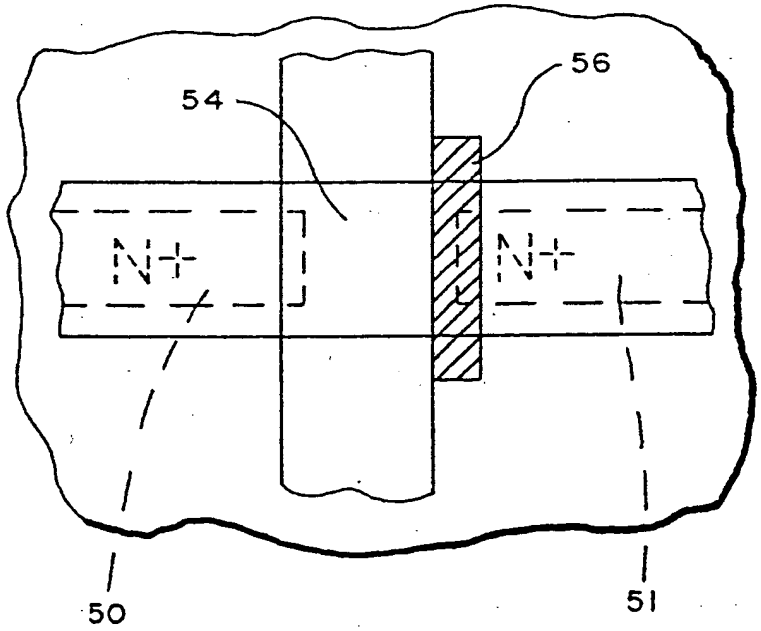

FIG.— 8

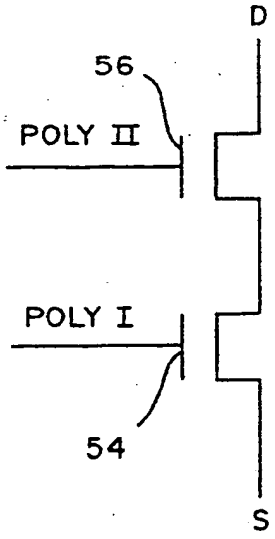

FIG.— 9

Nouvellement déposé

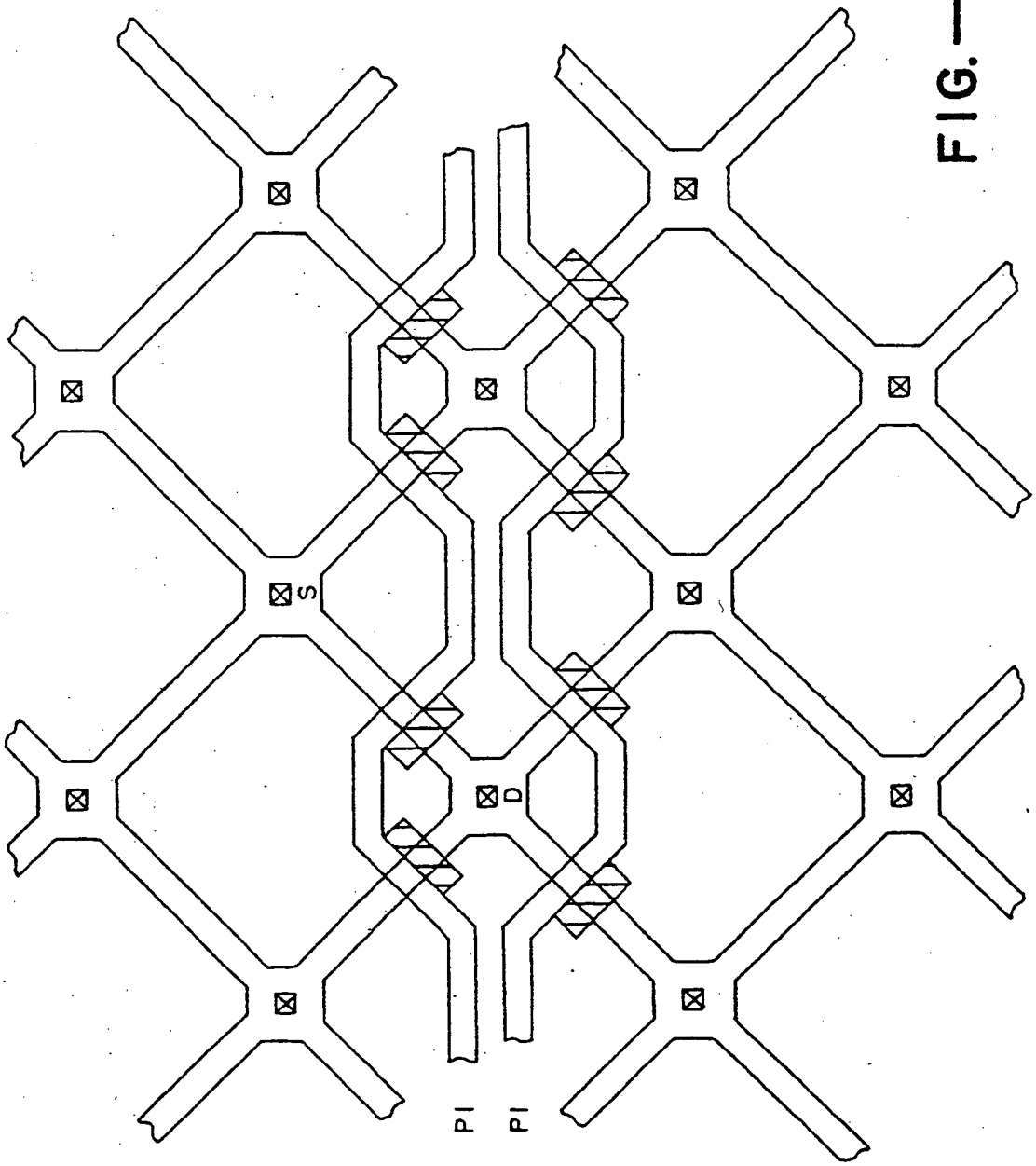

FIG. — 10

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 389 721 A3

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 89313498.1

(51) Int. Cl.5: H01L 29/788, H01L 21/28, //G11C17/00

(22) Date of filing: 22.12.89

(30) Priority: 27.03.89 US 328964

(43) Date of publication of application: 03.10.90 Bulletin 90/40

(84) Designated Contracting States: DE FR GB NL

(88) Date of deferred publication of the search report: 02.01.91 Bulletin 91/01

(71) Applicant: ICT INTERNATIONAL CMOS TECHNOLOGY, INC.
2125 Lundy Avenue
San Jose California 95131(US)

(72) Inventor: Wang, Samuel T.
1084 DiNapoli Drive
San Jose California 95129(US)

(74) Representative: Hardisty, David Robert et al
BOULT, WADE & TENNANT 27 Furnival Streeteet
London EC4A IPQ(GB)

(54) Flash EPROM cell and method of making such cell.

(57) A flash EPROM cell is fabricated using a two polysilicon enhancement mode n-channel transistor process. An active transistor region is formed in a silicon substrate (14) by growing a field oxide (16) around the region. A first polysilicon layer is deposited, etched, and oxidised to form an insulated control gate electrode (18). A second polysilicon layer is deposited over the active transistor region and the control gate electrode (18) and then anisotropically etched to remove all of the second polysilicon material except for a filament (20) adjacent to the control gate electrode (18), which forms a floating gate electrode (20). Source and drain regions (10, 12) are formed in the active transistor region with the control gate electrode (18) and the floating gate electrode (20) positioned over the channel region interconnecting the source and drain regions. The cell is programmed by hot electron channel current injection by proper voltage biasing of the control gate electrode (18) and drain (12). The cell can be either symmetrical or asymmetrical depending on the configuration of the floating gate filament electrode (20).

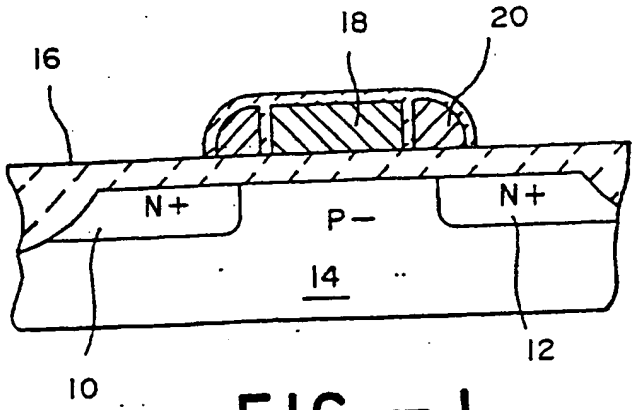

FIG.— 1

EP 0 389 721 A3

European Patent Office

PARTIAL EUROPEAN SEARCH REPORT

which under Rule 45 of the European Patent Convention shall be considered, for the purposes of subsequent proceedings, as the European search report

Application number

EP 89 31 3498

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 193 841 (K.K. TOSHIBA) * Page 6, line 1 - page 7, line 13; figures 2A-3G * --	1,10, 13,16	H 01 L 29/788 H 01 L 21/28// G 11 C 17/00
A	I.E.E.E. TRANSACTIONS ON ELECTRON DEVICES, vol. ED-34, no. 6, June 1987, pages 1297-1303, New York,US; Y. MIZUTANI et al.: "Characteristics of a new EPROM cell structure with a sidewall floating gate" * Whole article * --	1,10, 13,16	
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-16, no. 3, June 1981, pages 195-200, New York, US; ./.		TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L

INCOMPLETE SEARCH

The Search Division considers that the present European patent application does not comply with the provisions of the European Patent Convention to such an extent that it is not possible to carry out a meaningful search into the state of the art on the basis of some of the claims.

Claims searched completely: 1-10,13-17
Claims searched incompletely: 12
Claims not searched: 11
Reason for the limitation of the search:

Claim 11 is not disclosed.

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-10-1990	BAILLET

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1505.1 03.82

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
	B.GERBER et al.: "A 1.5. V single-supply one-transistor CMOS EEPROM" * Figure 1 *	1,2,9	
	--		
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-17, no. 5, October 1982, pages 852-856, New York, US; S. HIJIYA et al.: "A nitride-barrier avalanche-injection EAROM" * Figure 1 *	1,2,4	
	----		TECHNICAL FIELDS SEARCHED (Int. Cl.4)